



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/825,599

04/16/2004

Joon Kyu Park

049128-5148

8043

9629 7590 06/15/2007  
MORGAN LEWIS & BOCKIUS LLP  
1111 PENNSYLVANIA AVENUE NW  
WASHINGTON, DC 20004

EXAMINER

LEWIS, DAVID LEE

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

06/15/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/825,599

Applicant(s)

PARK, JOON KYU

Examiner

David L. Lewis

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 14 and 18 is/are rejected.
- 7) ☐ Claim(s) 2-13, 15-17 and 19-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 1. Claims 1, 14, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Bae et al. (6943760).**

**As in claim 1, Bae et al. teaches of a driving apparatus for an electro-luminescence display panel, figures 1-4, column 1 lines 10-15,**

**comprising: an electro-luminescent display panel having electro-luminescent light-emitting cells provided at crossings of gate lines and data lines, column 1 lines 10-15, column 2 lines 1-15, figures 1 and 2;**

**a current generating circuit that generates a current corresponding to an externally supplied digital data, figure 2 item reference block, figure 4 item I, column 4 lines 1-15;**

a data driver that samples the current from the current generating circuit for each horizontal period to generate a data voltage corresponding to the current and applies the generated data voltage to the data lines, **figure 1 item 15, figure 2 item 27, column 2 lines 1-15, column 4 lines 1-15 and 55-60**, wherein said horizontal period is inherent to the data clock 22 as known in the art, wherein the digital signals are received from the external source according to the known horizontal and vertical signals in the data clock 22 to provide information to the matrix display and sampled according to a switch S1

and a timing controller that controls the data driver, applies the digital data to the current generating circuit, and generates a sampling control signal for controlling the data driver to apply the sampled signal to the data driver, **figure 1 item 17, figure 4 item S1, column 5 lines 1-5**.

**As in claim 14, Bae et al. teaches of a method of driving an electro-luminescence display panel, figures 1-4, column 1 lines 10-15,**

comprising the steps of: preparing an electro-luminescent display panel having electro-luminescent light-emitting cells provided at crossings of gate lines and data lines, **column 1 lines 10-15, column 2 lines 1-15, figures 1 and 2;**

generating a current corresponding to an externally provided digital data, **figure 2 item reference block, figure 4 item I, column 4 lines 1-15;**

Art Unit: 2629

sampling the current during each horizontal period to generate and store the data voltage corresponding to the current, **figure 1 item 15, figure 2 item 27, column 2 lines 1-15, column 4 lines 1-15 and 55-60**, wherein said horizontal period is inherent to the data clock 22 as known in the art, wherein the digital signals are received from the external source according to the known horizontal and vertical signals in the data clock 22 to provide information to the matrix display and sampled according to a switch S1, wherein the memory unit 12 stores the image signal corresponding to the digital information that produces said current and voltage;

applying the stored data voltage to the data lines, **column 4 lines 50-60**;

and driving the light-emitting cells using the data voltage, **column 4 lines 1-25 and 50-60**.

**As in claim 18, Bae et al. teaches of a method of fabricating an electro-luminescent display panel, figures 1-4, column 1 lines 10-15,**

comprising the steps of: providing an electro-luminescence display panel having electro-luminescent light-emitting cells arranged at crossings of gate lines and data lines, **column 1 lines 10-15, column 2 lines 1-15, figures 1 and 2**;

providing a current generating circuit for generating a current corresponding to a digital data from the exterior, **figure 2 item reference block, figure 4 item I, column 4 lines 1-15**;

and providing a data driver for sampling the current from the current generating circuit for each horizontal period, for generating the data voltage corresponding to the current, and for applying the data voltage to the data lines at one side of a substrate, **figure 1 item 15, figure 2 item 27, column 2 lines 1-15, column 4 lines 1-15 and 55-60**, wherein said horizontal period is inherent to the data clock 22 as known in the art, wherein the digital signals are received from the external source according to the known horizontal and vertical signals in the data clock 22 to provide information to the matrix display and sampled according to a switch S1, wherein the memory unit 12 stores the image signal corresponding to the digital information that produces said current and voltage.

### ***Allowable Subject Matter***

2. Claims 2, 15, 19 and therefore claims 2-13, 15-17 and 19-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach of said limitations of claims 2, 15, and 19.

### ***Conclusion***

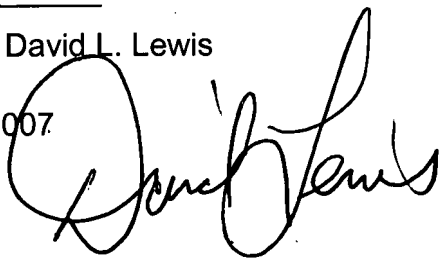
3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. 2004/0095304, 2004/0036664, 7102600, 20030189541

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.
5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

---

Examiner: David L. Lewis

June 10, 2007

A handwritten signature in black ink, appearing to read "David L. Lewis", is written over the printed name and date.